What is claimed is:

1. A buffer control apparatus in a buffered switch for controlling transmission of packets/frames of data, comprising:

a dual port buffer memory for storing the packets/frames of data;

a buffer write module for writing packets/frames into the dual port buffer memory;

a buffer read module for reading packets/frames of data from the dual port buffer memory; and

a deferred queue device for controlling the buffer read module so as to temporarily defer transmission of the packets/frames to a destination port which is unavailable to receive the packets/frames.

2. The buffer control apparatus according to claim 1, wherein the deferred queue device queues packets/frames which can not be transmitted to destination ports which are unavailable.

3. The buffer control apparatus according to claim 1, wherein the deferred queue device comprises:

a deferred header queue device for storing frame information for packets/frames being deferred;

means for periodically determining current status of all destination ports in the buffered switch; and

header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port.

4. The buffer control apparatus according to claim 3, wherein the deferred queue device is in one of an Initial State, a Deferred State, and a Backup State.

5. The buffer control apparatus according to claim 3, wherein the buffer control device further comprises:

a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port.

6. The buffer control apparatus according to claim 3, wherein the buffer control device further comprises:

a backup header queue device that operates in parallel with the deferred header queue for storing frame information for packets/frames waiting to be sent to at least destination port.

7. The buffer control apparatus according to claim 3, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch.

8. The buffer control apparatus according to claim 3, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

9. The buffer control apparatus according to claim 5, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

10. A deferred queue device for temporarily deferring transmission of packets/frames to a destination port in a buffered switch, comprising:

a deferred header queue device for storing frame information for packets/frames being deferred;

means for periodically determining current status of all destination ports in the buffered switch; and

header select logic unit for determining state of the deferred queue device and supplying a valid buffer address for a deferred packet/frame which can now be sent to an available destination port.

11. The deferred queue device according to claim 10, wherein the deferred queue device can be in one of an Initial State, a Deferred State, and a Backup State.

12. The deferred queue device according to claim 10, further comprising:

a backup header queue device for storing frame information for packets/frames waiting to be sent to at least one destination port because the

packets/frames arrived at an input port while deferred packets/frames were being sent to the at least one destination port.

13. The deferred queue device according to claim 10, further comprising:

a backup header queue device that operates in parallel with the deferred header queue for storing frame information for packets/frames waiting to be sent to at least destination port.

14. The deferred queue device according to claim 10, wherein XOFF masks are used to determine current status of all destination ports in the buffered switch.

15. The deferred queue device according to claim 10, wherein the deferred queue device queues packet/frames which can not be transmitted to the destination ports.

16. The buffer control apparatus according to claim 10, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

17. The buffer control apparatus according to claim 12, wherein the stored frame information comprises frame header information and a starting address in the buffer memory for the packet/frame.

18. A method for temporarily deferring transmission of packets/frames to a destination port in a buffered switch, comprising the steps of:

receiving a request for transmission of at least one packet/frame to the destination port;

determining whether the destination port is available to receive the at least one packet/frame;

deferring transmission of the at least one packet/frame when the destination port is not available to receive the at least one packet/frame; and

repeating the above steps for a next packet/frame to be transmitted.

19. The method according to claim 18, further comprising the steps of:

storing a frame /packet identifier and memory address for each deferred packet/frame in a deferred header queue;

periodically checking to determine if destination ports for deferred packets/frames are available;

transmitting the at least one packet/frame to destination ports when it is determined that the destination ports are available; and

removing frame/packet identifier and memory address for the at least one transmitted packet/frame from the deferred header queue.

20. The method according to claim 19, wherein each frame/packet identifier and memory address is stored in the same order it was received.

21. The method according to claim 20, wherein each frame/packet is transmitted to the destination port based on the oldest packet identifier at the deferred header queue for the destination port.

22. The method according to claim 18, further comprising the step of:

transmitting the at least one packet/frame to the destination port if it is determined that the destination port is available.

23. The method according to claim 19, further comprising the steps of:

storing packet/frame identifier and memory address in a backup header queue for packets/frames which are received while a deferred packet/frame is being sent to the destination port;

periodically checking to determine if the destination ports for packets/frames in the backup header queue are available;

transmitting the packets/frames to the destination ports when it is determined that the destination ports are available;

removing frame/packet identifier and memory address for transmitted packets/frames from the backup header queue.

24. The method according to claim 23, wherein each frame/packet identifier is transmitted to the destination port based on first packet received at the backup header queue for the destination port.